In re Patent Application of:
BAHOUT
Serial No. **10/081,740**
Filing Date: **FEBRUARY 22, 2002**

In the Claims:

Claims 1 to 6 (Cancelled).

7. (Previously Presented) A method of reading sequentially from a memory having an incremental address counter associated therewith, the method comprising:

detecting an address jump signal;

incrementing the incremental address counter based upon the detected address jump signal;

reading a content of the memory at the incremented address;

transferring the content read at the incremented address to the incremental address counter; and

reading the content of the memory at the address contained in the incremental address counter.

8. (Previously Presented) A method according to Claim 7, wherein detecting an address jump signal comprises decoding an instruction code.

9. (Previously Presented) A method according to Claim 7, wherein the incremental address counter is incremented by at least one unit.

10. (Previously Presented) A method according to Claim 7, wherein transferring the content read comprises transferring a memory address code corresponding to a following address.

11. (Currently Amended) A method for reading

sequentially from a memory, the method comprising:

providing an instruction code and a memory address code to an input register;

providing the memory address code to an incremental address counter having an input connected to the input register and an output connected to the memory;

reading the memory ~~read~~ at the memory address code indicated by the incremental address counter;

recording contents read from the memory in an output register;

detecting an address jump instruction code using an address jump detection circuit having an input connected to the input register, and an output connected to the incremental address counter;

providing an increment signal from the address jump detection circuit output connected to the incremental address counter based upon the detected address jump instruction code; and

transferring the recorded contents read at the incremented address to the incremental address counter.

12. (Currently Amended) A method according to Claim 11, wherein the recorded contents ~~comprises~~ comprise a memory address code corresponding to a following address.

13. (Previously Presented) A method according to Claim 11, wherein the incremental address counter is incremented by at least one unit.

14. (Previously Presented) A method according to

In re Patent Application of:
BAHOUT
Serial No. **10/081,740**
Filing Date: **FEBRUARY 22, 2002**

Claim 11, wherein the address jump detection circuit comprises a decoder circuit.

15. (Previously Presented) A method according to Claim 11, wherein the transferring is performed using a transfer circuit connected to the incremental address counter and to the output register.

16. (Currently Amended) A method according to Claim 15, wherein the transfer circuit comprises:

a logic gate having an input connected to the output register for transferring in parallel the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of the logic gate, and an output connected to the incremental address counter for directing thereto either the ~~memory address code~~ recorded contents in the input register or the memory address code at the incremented address.

17. (Previously Presented) A device for reading sequentially from a memory, the device comprising:

an input register containing an instruction code and a memory address code;

an incremental address counter having an input connected to said input register for receiving the memory address code therefrom, and an output connected to the memory;

an output register having an input connected to the memory for recording contents read at the memory address code indicated by said incremental address counter;

an address jump detection circuit having an input connected to said input register for detecting an address jump instruction code, and an output connected to said incremental address counter for supplying an increment signal thereto; and

a transfer circuit connected to said incremental address counter and to said output register for transferring the recorded contents read at the incremented address to said incremental address counter.

18. (Previously Presented) A device according to Claim 17, wherein the recorded contents comprises a memory address code corresponding to a following address.

19. (Previously Presented) A device according to Claim 17, wherein said address jump detection circuit comprises a decoder circuit.

20. (Previously Presented) A device according to Claim 17, wherein said transfer circuit comprises:

a logic gate having an input connected to said output register for transferring in parallel the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of said logic gate, and an output connected to said incremental address counter for directing thereto either the memory address code in said input register or the recorded contents at the incremented address.

21. (Previously Presented) A device for reading

sequentially from a memory, the device comprising:

an input register containing an instruction code and a memory address code;

an incremental address counter having an input connected to said input register for receiving the memory address code therefrom, and an output connected to the memory;

an output register having an input connected to the memory for recording contents read at the memory address code indicated by said incremental address counter;

an address jump detection circuit having an input connected to said input register for detecting an address jump instruction code, and an output connected to said incremental address counter for supplying an increment signal thereto;

a logic gate having an input connected to said output register for transferring the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of said logic gate, and an output connected to said incremental address counter for directing thereto either the memory address code in said input register or the recorded contents at the incremented address.

22. (Previously Presented) A device according to Claim 21, wherein the recorded contents comprises a memory address code corresponding to a following address.

23. (Previously Presented) A device according to Claim 21, wherein said address jump detection circuit comprises a decoder circuit.

24. (Previously Presented) A device according to Claim 21, wherein said logic gate transfers the contents from the memory to said multiplexer circuit in parallel.

25. (Previously Presented) A device comprising:

a microprocessor;

an input register connected to said microprocessor for receiving an instruction code and a memory address code therefrom;

an incremental address counter having an input connected to said input register for receiving the memory address code therefrom;

a memory having an input connected to an output of said incremental address counter;

an output register having an input connected to said memory for recording contents read at the memory address code indicated by said incremental address counter;

an address jump detection circuit having an input connected to said input register for detecting an address jump instruction code, and an output connected to said incremental address counter for supplying an increment signal thereto; and

a transfer circuit connected to said incremental address counter and to said output register for transferring the recorded contents read at the incremented address to said incremental address counter.

26. (Previously Presented) A device according to Claim 25, wherein the recorded contents read at the memory address code indicated by said incremental address counter are

read sequentially from said memory.

27. (Previously Presented) A device according to Claim 25, wherein the recorded contents comprises a memory address code corresponding to a following address.

28. (Previously Presented) A device according to Claim 25, wherein said address jump detection circuit comprises a decoder circuit.

29. (Previously Presented) A device according to Claim 25, wherein said transfer circuit comprises:

a logic gate having an input connected to said output register for transferring in parallel the contents therefrom corresponding to the recorded contents at the incremented address; and

a multiplexer circuit having an input connected to an output of said logic gate, and an output connected to said incremental address counter for directing thereto either the memory address code in said input register or the recorded contents at the incremented address.